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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,423	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-22 and 24-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-22 and 24-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-12, 14-22 and 24-40 remain for examination.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. Claims 1-8, 14-22 and 24-31 are rejected under 35 USC § 103 as being unpatentable over Steinmetz et al., U.S. patent 5,485,624.

Steinmetz et al. taught (e.g. see figs. 1-6) the invention substantially as claimed (as per claim 1), including a data processing ("DP") system comprising:

A. a method of performing data string operations (col. 2 lines 13-17) comprising;

B. routing a series of instructions (col. 1 lines 52-53) to a microprocessor (fig. 2, 12, 13) having a first execution unit for executing instructions (all processors inherently have at least a first execution unit for executing instructions);

C. analyzing said series of instructions so as to detect an instruction to perform a data string operation (col. 2 line 65 to col. 3 line 2);

D. routing said instruction to perform a data string operation to a second execution unit (fig. 2, 11) separate from said first execution unit (col. 1 lines 49-52, col. 2 lines 13-17, by performing the data string operations transparently to the primary processor which does not natively support co-processing, Steinmetz et al. is indicating that the second processor is separate from the first processor's execution unit), wherein said second execution unit receives an undecoded version of said instruction (fig. 2 shows that the second processor connects to lines 12 and 13 and so receives the instructions from memory as the are read from memory, before they are decoded by the first processor 14);

E. controlling read and write operations to and from external memory with said first execution unit via control circuitry and without intervention by said second execution unit (fig. 2 shows that the first processor (14) is connected directly to the memory (10) and as such controls the memory without intervention by the second execution unit

(11)), wherein said external memory is external to said general purpose microprocessor (fig. 2 shows that the memory (10) is external to both the first processor (14) and the second processor (11); and,

F. controlling read and write operations to and from external memory with said second execution unit via control circuitry (fig. 2 shows that the second processor (11) is connected directly to the memory (10) via lines (12) and (13)) and without intervention by said first execution unit (fig. 2 shows that second processor (11) controls memory (10) directly, without assistance by the first processor (14). Furthermore, col. 2 lines 13-17 indicate that the second processor sets up and performs data string operations transparently to the first processor. Performing the operations transparently equates to performing them without intervention by the first processor).

4. Steinmetz et al.'s exemplary embodiment did not detail that the first processor (14) was a general purpose processor. However, Steinmetz et al. did indicate to one of skill in the art that his invention was applicable to general purpose processors (col. 1 lines 15-19). Accordingly, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have utilized Steinmetz et al.'s invention in a system containing a general purpose processor because of Steinmetz et al.'s indication that his invention was useful to add to a general purpose processor to increase the efficiency with which the system can perform tasks that the general purpose processor is not itself efficient at performing.

5. As to claim 2, Steinmetz et al. taught that the first execution unit was on a first integrated circuit and that the second execution unit was on a second integrated circuit (at col. 1 lines 30-45 and col. 2 lines 56-58 Steinmetz et al. indicates that the primary processor is a standard 53C710 SCSI I/O processor available from the NCR corporation. Accordingly, this indicates that in Steinmetz et al. embodiment the primary processor was one integrated circuit chip purchased from the NCR corporation, and accordingly the second processor must have been placed upon a second integrated circuit chip).

6. As to claim 3, Steinmetz et al. taught that the second integrated circuit chip included a bus interface unit in association with the second execution unit (col. 2 lines 65-66, the EISA bus that the second processor interfaces with shows that the second processor contains a "bus interface unit" for the EISA bus).

7. As to claim 4, Steinmetz et al. taught that the second integrated circuit comprised a memory controller (col. 2 lines 65-66, since the second processor controls data string operations with the memory 10, it must additionally comprise a memory controller to control accesses to the memory).

8. As to claim 5, Steinmetz et al. taught that the act of routing the data string instruction to the memory controller comprised writing the data string instruction to an I/O address (col. 2 line 66 to col. 3 line 19).

9. As to claim 6, Steinmetz et al. taught that the I/O address was normally not used for I/O devices (col. 3 lines 5-7).

10. As to claim 7, Steinmetz et al. did not teach a cache. However, at the time of applicant's invention, it was very well known to provide a cache for the purpose of enhancing performance of the system and official notice of such is hereby taken. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have included a cache in any system built based upon the teachings of Steinmetz et al. because of this increased performance. Once one of skill in the art adds a cache to the system, it becomes inherent that the system must consult the cache for data to maintain memory coherency.

11. As to claim 8, once a cache is added to the system, it becomes inherent that modified data within that data cache will be flushed to main memory before or during the operation of a data string instruction in order to maintain memory coherency.

12. As to claims 14-22 and 24-31 they do not teach or define above the invention claimed in claims 1-8 and are therefore rejected under Steinmetz et al. for the same reasons set fourth in the rejection of claims 1-8, supra.

13. Claims 9 and 32 are rejected under 35 USC 102(b) as being clearly anticipated by

Imamura et al., U.S. Patent 5,134,698.

14. Claims 10-12, 38-40 rejected under 35 USC § 103 as being unpatentable over Imamura et al., U.S. patent 5,134,698.

15. Claims 33-37 are rejected under 35 USC § 103 as being unpatentable over Imamura et al., U.S. patent 5,134,698, in view of Young et al., U.S. Patent 5,548,730.

16. The rejections of claims 9-12 and 32-40 are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 20060620, mailed June 28, 2006.

17. Applicant's arguments filed September 29, 2006, have been fully considered but they are not deemed to be persuasive.

18. In the remarks, applicant argues in substance:

A. That: "Independent Claim 9 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent claim 1"

"Independent Claim 32 is believed to be patentably distinguished over the cited art for reasons similar to those set forth above with respect to the patentability of amended independent Claim 1"

This is not found persuasive because the claim limitations for which applicant argues patentability of claim 1, that the first and second execution units control read and write operations to the memory without intervention by each other and that the second execution unit receives an undecoded version of the data string operation instruction do not exist in either of claims 9 or 32. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

> "It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).
>
> "The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

B. That (in regards to claim 9): "Imamura does not appear to disclose a processing system having "memory circuitry ... configured to be alternatively controlled by [a] first execution unit and [a] second execution unit using the same memory control circuitry, wherein said first [and] second execution unit[s] are separately coupled to said memory control circuitry."

This is not found persuasive because as is seen from fig. 1 of Imamura et al. there is disclosed "memory circuitry" (4, 5) which is "configured to be alternately controlled by a first execution unit (1) and a second execution unit (2) using the same memory control circuitry" (both 1 and 2 are connected to the same memory, therefore, to the same memory control circuitry) wherein the "first and second units are separately coupled to said memory control circuitry' (IP 1 is connected through SC 2 to MS 4 which is a separate connection from the direct connection of SC 2 to MS 4 and ES 5).

C. That (in regards to claim 32): "Imamura does not appear to disclose a method including "routing a series of instructions to a general purpose microprocessor having a first execution unit; analyzing said series of instructions so as to detect an instruction to perform a data string operation; and routing said instruction to perform a data string operation to a second execution unit such that said first execution unit does not receive said instruction."

This is not found persuasive because as to the quoted claimed steps of routing, first execution unit, analyzing to detect, and routing said instruction, those elements were clearly shown as present in Imamura et al. in paper number 20060620, mailed June 28, 2006. As to

the claim limitation that the first execution unit does not receive said instruction, that aspect is found in Imamura et al. at col. 5 lines 11-14 where Imamura et al. clearly details that the data transfer instruction is detected and routed from IP 1 to SC 2. Because of this detection and routing, and because this instruction is intended to cause SC 2 to perform a data string operation, Imamura et al. has indicated that the execution unit of IP 1 does not receive the instruction for execution. I.e., the instruction is executed by SC 2, and is therefore not executed by IP 1.

19. Applicant's arguments with respect to claims 1-8, 14-22 and 24-31 have been considered but are deemed to be moot in view of the new grounds of rejection.

20. Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

21. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
December 11, 2006

RICHARD L. ELLIS
PRIMARY EXAMINER